In the Specification

The specification has been amended as follows:

Amend the paragraph beginning at page 3 line 4 as follows:

The above and other objects and advantages, which will be apparent to one of skill in the art, are achieved in the present invention which is directed to, in a first aspect, ~~to~~ a method of forming an isolation in a semiconductor substrate comprising providing a semiconductor substrate, forming a plurality of adjacent trenches, preferably vertical deep trenches, in the semiconductor substrate leaving adjacent segments of the semiconductor substrate between each of the adjacent trenches, and depositing a barrier layer in the plurality of adjacent trenches. Subsequently a portion of the barrier layer in each of the plurality of adjacent trenches is removed to expose portions of the adjacent segments of the semiconductor substrate, and such exposed portions of the adjacent segments of the semiconductor substrate are merged together to form a self-aligned shallow trench isolation.

Amend the paragraph beginning at page 8 line 12 as follows:

Fig. 11 is a partial cross-sectional view of Fig. 10 showing the buried strap connection having a trench-top oxide provided thereover the substrate and a transistor gate dielectric in the trenches, along a sidewall of the upper region of the trench, thereby being in direct contact with the exposed portions of ~~substrate~~the substrate.

Amend the paragraph beginning at page 15 line 15 as follows:

Fig. 5 illustrates the merged thermal oxide regions 30 from a top plane view of a partial horizontal cross-sectional view of the cut plane indicated by the dashed line 40 in Fig. 4. As shown in Fig. 5, the thermal oxide regions 30 merge together, as indicated by dashed lines 34, along adjacent trenches 18 along selected orientations of single paths or rows ~~42~~ of trenches 42 to provide the continuous self-aligned shallow trench isolation structure which eliminates the need for an isolation mask to separate adjacent rows of trenches 42. In the preferred embodiment, as illustrated in Fig. 5, the trenches 18 within a single row 42 are closer to each other in comparison to trenches along the adjacent active area rows 45. Furthermore, as depicted by dashed line 34 in Figs 4 and 5 illustrating the merged, self-aligned thermal oxide regions 30 of a single row of trenches 42, the merged self-aligning thermal oxide isolation regions 30 merge together both vertically and horizontally to provide the continuous, merged, self-aligned thermal oxide region 30 which surrounds each trench 18 of the plurality of trenches along each path of trenches 42 on the substrate.

Amend the paragraph beginning at page 16 line 1 as follows:

Further as shown in Fig. 5, remaining portions of silicon substrate 10, which were not oxidized during the process of converting the thin silicon portions 12 into the merged self-aligning thermal oxide isolation regions 30, exist between the

adjacent active area rows 45 on the substrate 10. The remaining portions of silicon substrate 10 provides a continuous region of silicon substrate 10 between the adjacent active area rows ~~45,thereby~~45, thereby providing electrically continuous regions of silicon substrate between such adjacent active area rows 45 in which transistors may subsequently be formed by techniques as known and used in the art. See Fig. 5. Therefore in the present invention, the self-aligned, merged thermal oxide regions 30 electrically isolate a current between adjacent rows of silicon substrate 10 existing between the adjacent active area rows 45, without requiring the additional processing steps, such as ~~an~~ isolation masks, needed to separate the adjacent active area rows 45. In the preferred embodiment, the continuous, merged self-aligned thermal oxide regions 30 along paths of trenches 42 isolate, or block electrical conduction between adjacent rows of silicon substrate 10 existing therebetween the adjacent active rows 45.

Amend the paragraph beginning at page 16 line 16 as follows:

Thus, the present invention provides a self-aligned shallow trench isolation structure by converting the thin regions of silicon substrate 12 between adjacent trenches into thin oxidized, merged regions of silicon substrate for isolating various transistors within a memory array automatically thereby aligning and defining the location of the isolation region. In the present invention, the thin thermal silicon dioxide regions 30 are self-aligned, as-formed, as a result of the thin silicon substrate portions 12 being simultaneously oxidized and merged between adjacent

trenches along a path of trenches 42 in the same process to automatically ~~aligned~~ ~~the~~align edges of the thin thermal silicon dioxide regions 30 to the as-formed, original outer edges of the deep trenches 18. Thus, the edges of the thin thermal silicon dioxide regions 30 directly contact the as-formed, original outer edges of the deep trenches 18 to fill any gaps between the thin thermal silicon dioxide regions and the trenches 18. As such, the present invention eliminates the need for additional masking processes for defining the location of the isolation region.